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EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,468	ABE, OSAMU	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *May 20, and Jun 17, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,6,8-10,12-17 and 19-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,6,8-10,12-17 and 19-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER
8/8/05

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06172005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/IDS

The amendment submitted on May 20, 2005, and the IDS submitted on Jun 17, 2005, were reviewed and considered with the following results:

The objection to the specification, as described on page 3 of the previous Office Action was apparently not addressed. Therefore, that objection has been maintained and is repeated later under the appropriate section.

Cancelled claim 2 rendered its prior art rejection moot.

Claims 4, 7, 11, and 18 were also cancelled, wherein their recited material, previously described as allowable in the previous Office Action, was entered into corresponding claims.

Therefore, amended claims 1, 3, 5, 10, 12, 17, and 19 overcame all the prior art rejections described in the previous Office Action, which have now been withdrawn. Those rejections include: 1) claims 1, 3, 10, and 13-14 under 35 U.S.C. 102(b) with respect to McNeill et al.; 2) claims 1 and 10 under 35 U.S.C. 102(b) with respect to Tokuda; 3) claims 3, and 13-14 under 35 U.S.C. 103(a) with respect to Tokuda/Oda; 4) claims 8 and 16 under 35 U.S.C. 103(a) with respect to Tokuda; and 5) claims 5-6, 9, 17, 20, and 22 under 35 U.S.C. 103(a) with respect to Tokuda/Oda. None of these references clearly shows or discloses the second element, having a capacitive component, comprising an ion implantation resistor as now recited within independent claims 1 and 5, or the voltage supply circuit comprising the constant current source, and either first/second transistors or first/second pairs of cascaded transistors, as now recited within independent claims 10, 12, 17, and 19.

However, after reconsidering the amended claims, and the applicant's prior art reference cited on the IDS submitted Jun 17th, new claim objections and rejections were noted based on two observations: 1) the actual relationships between the first/second elements and the other elements recited within the circuit are confusing; and 2) the prior art reference shows two related figures that closely correspond to the basic structure shown in the applicant's own Fig. 1, therefore providing reasoning to reconsider, and reject, most of the present application's claims, including the newly added claims. Therefore, the allowable material in some of the claims, as described in the previous Office Action, has also been withdrawn. The new objections and rejections are described later under the appropriate section.

This action is NON-FINAL since the previous Office Action has indicated allowability of claims that are now rejected, and the amended claims had also overcome all the rejections described in that action.

Specification

The amended "paragraph commencing at page 3, line 24" on page 2 of the Nov 18th amendment is objected to because of the following informalities: Since the amended change is not clearly shown, it is suggested that paragraph be re-submitted with the intended change identified. Also, it is suggested the phrase --gate of-- be added after "has the" on line 4 of the paragraph to more clearly identify what is actually connected between P2 and N2. An appropriate correction is required.

Claim Objections

Claims 1, 3, 5-6, 8-10, 12-17, and 19-29 are objected to because of the following informalities: Line 10 of both independent claims 1 and 5, and line 11 of independent claims 10,

12, 17, and 19 should have "the" deleted from "the potential" since that potential had not been previously identified. Claims 1 (line 16), 5 (line 15), 13 (line 4), 17 (line 16), 19 (line 16), and 23 (line 4) should have --source-- added after "voltage" to provide consistent labeling throughout the claims (e.g. see "power supply voltage source" cited previously in the (associated) independent claim) to minimize possible confusion. Dependent claims carry over any objection(s) from any claim(s) upon which they depend. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3, 5-6, 8-9, 13-15, 17, and 19-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The limitations of the first circuit and the second element within claims 1 and 5 are misleading. As presently written, it appears that the second element of claim 1 (see lines 14-17), and claim 5 (lines 16-18), is separate from the other elements recited (e.g. the first circuit cited on line 6 of both claims 1 and 5). However, isn't the second element actually part of the first circuit (e.g. see second element R2 in first circuit R1-R3,D1-D2 of the applicant's own Fig. 1)? For similar reasons, it is believed the first/second elements of claims 13, 17, 19, and 23 are part of the voltage supply circuit/first circuit, respectively recited within claims 10, 17, 19, and 12. For example, each of claims 13 and 23 cites "further comprising", thus implying the first/second elements are separate, distinct elements from those already recited within their respective independent claim. Similarly, the limitations recited within each of claims 17, and 19 also imply the voltage supply circuit, first circuit, and

first/second elements are all distinct elements. Therefore, changes and/or clarification are requested to clearly describe how the second element, and/or the first element, relates to any of the other recited items within their corresponding independent claim.

Related to the rejections described above, claims 1, 13, and 23 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are how the first and second elements relate to any of the previously recited items within the claim (e.g. amplifier, first circuit, switching element, and circuit output terminal).

Dependent claims carry over any rejection(s) carried over from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 10, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kraus et al. (Kraus), a reference found during the recent update search, wherein this reference corresponds to the Taiwan patent 210414 cited on the applicant's IDS. Fig. 2 shows a band gap circuit, with Fig. 4 showing an example of a basic CMOS operational amplifier that can be used as OP within Fig. 2 (e.g. see column 3, lines 18-25). Therefore, one of ordinary skill in the art would understand the band gap circuit comprises voltage supply circuit IO,M6-M8 (see Fig. 4)

connected to power supply voltage source VDD; reference potential point VSS; circuit output terminal VR connected to the voltage supply circuit; differential amplifier M1-M4 (see Fig. 4) connected to the voltage supply circuit, and having inverting/noninverting input terminals VN/VP (e.g. see column 5, lines 62-65), and an output terminal (not labeled but understood to be the common connection between M2 and M4); first circuit R1-R3,T1-T2 (see Fig. 2) for causing a potential difference to occur at the inverting/noninverting input terminals VN/VP in response to fluctuation of voltage VR on circuit output terminal VR; and switching element M5 (see Fig. 4) that will allow excess current from circuit output terminal VR to flow to reference potential point VSS in response to fluctuation of the differential amplifier's output terminal, wherein switching element M5 is connected to circuit output terminal VR, reference potential point VSS, and the differential amplifier's output terminal. The voltage supply circuit comprises constant current source IO,M6 (e.g. understood from the disclosure on column 6, lines 12-15, and 59-63); first transistor M7 coupling the differential amplifier to power supply voltage source VDD and the constant current source; and second transistor M8 coupling circuit output terminal VR to power supply voltage source VDD and the constant current source. Therefore, claim 10 is anticipated. Since switching element M5 is an N-channel MOS transistor, claim 16 is also anticipated.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus as applied to claim 10 above, and further in view of Oda, a reference cited in the previous Office Action. As previously described, Kraus shows a band gap circuit in Fig. 2 having operational amplifier OP, with an example of a basic CMOS operational amplifier shown in Fig. 4, wherein an understanding of these figures meet the limitations of claim 10 as previously described. However, the reference does not clearly show or disclose first/second elements with resistive/capacitive components, respectively for removing power supply noise. Fig. 1 of Oda shows first element R1 with resistive component R1, and second element C1-C2 with capacitive component C1-C2, coupled to the output of a reference voltage generating source. The first/second elements remove noise at the output (e.g. see column 1, lines 29-33 and 38-42). Therefore, it would have been obvious to one of ordinary skill in the art to apply Oda's R1,C1-C2 filter to the output of Kraus' band gap circuit, another known type of reference voltage generating source. The first/second elements, with their corresponding resistive/capacitive components, will help remove supply noise with respect to power supply voltage VDD. Therefore, claim 13 is rendered obvious. Although R1 of Oda is shown as a resistor, it also would have been obvious to one of ordinary skill in the art to replace first element R1 with a transistor functioning as a resistive component, thus rendering claim 14 obvious. The transistor could be used to provide a means for adjusting the resistive component of first element R1, thus allowing the operator to change the filtering characteristics of the first/second elements to meet the desired needs the circuit is being used in.

Applying the same type of reasoning as described above with a respect to independent claim 10 and its dependent claims 13-14 and 16, independent claim 17 and its dependent claims

20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus, in view of Oda. Claim 17 recites the basic limitations as recited within independent claim 10, plus the limitations of claim 13, which depends on claim 10. Therefore, all of the limitations recited within independent claim 17 correspond to those recited within the combination of independent claim 10 and its dependent claim 13 rejected above. Claim 20 recites the same limitation as claim 14 (i.e. the first element comprises a transistor), and claim 22 recites the same limitation as claim 16 (i.e. the switching element is an N-channel MOS transistor). Therefore, claims 17, 20, and 22 are rendered obvious for the same reasons as described above with respect to corresponding claims 10, 13, 14, and 16.

Claims 12 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al. (Kraus), and the knowledge of one of ordinary skill in the art. Fig. 2 of Kraus shows a band gap circuit with operational amplifier OP, wherein Fig. 4 shows an example of a basic CMOS operational amplifier that can be used as OP within Fig. 2 (e.g. see column 3, lines 18-25). Therefore, one of ordinary skill in the art would understand the band gap circuit comprises voltage supply circuit IO,M6-M8 (see Fig. 4) connected to power supply voltage source VDD; reference potential point VSS; circuit output terminal VR connected to the voltage supply circuit; differential amplifier M1-M4 (see Fig. 4) connected to the voltage supply circuit, and having inverting/ noninverting input terminals VN/VP (e.g. see column 5, lines 62-65), and an output terminal (not labeled but understood to be the common connection between M2 and M4); first circuit R1-R3,T1-T2 (see Fig. 2) for causing a potential difference to occur at the inverting/ noninverting input terminals VN/VP in response to fluctuation of voltage VR on circuit output terminal VR; and switching element M5 (see Fig. 4) that will allow excess current from circuit

output terminal VR to flow to reference potential point VSS in response to fluctuation of the differential amplifier's output terminal, wherein switching element M5 is connected to circuit output terminal VR, reference potential point VSS, and the differential amplifier's output terminal. The voltage supply circuit comprises constant current source IO,M6 (e.g. understood from the disclosure on column 6, lines 12-15, and 59-63); first transistor M7 coupling the differential amplifier to power supply voltage source VDD and the constant current source; and second transistor M8 coupling circuit output terminal VR to power supply voltage source VDD and the constant current source. However, the reference does not show or disclose first/second pairs of cascaded transistors, which would correspond to transistors M7/M8. It would have been obvious to one of ordinary skill in the art to add another current mirror cascoded with respect to current mirror M6-M8 of Kraus. With a pair of cascoded current mirrors, first transistor M7 and a corresponding transistor would be coupled in series between VDD and the differential amplifier, and second transistor M8 and its corresponding transistor would be coupled in series between VDD and circuit output terminal VR. These sets of series coupled transistors would be considered first/second pairs of cascaded transistors, thus rendering claim 12 obvious. Cascoded current mirrors are one way to help provide a stabilized output current, and by adding an additional transistor (e.g. one type of resistive device) within each current path, the circuit could operate from a higher power supply voltage source, provide a more stable current, and/or generate a lower output voltage because of the large voltage drop between VDD and VR. Since switching element M5 is an N-channel MOS transistor, claim 26 is rendered obvious.

Claims 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus as applied to claim 12 above, and further in view of Oda. As previously described, cascaded pairs

of transistors (e.g. associated with cascoded current mirrors) can be used within the voltage supply circuit. However Kraus does not show the first/second elements for removing power supply noise. Applying the same reasoning as described above in related rejections, it would have been obvious to one of ordinary skill in the art to use first element R1 and second element C1-C2 of Oda at the output of Kraus' band gap circuit, thus rendering claim 23 obvious. Replacing first element R1 with a transistor to allow means to adjust the filtering characteristics of the first/ second elements, renders claim 24 obvious.

Claims 19, 27, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus, in view of Oda and the knowledge of one of ordinary skill in the art. Applying the same type of reasoning as described above with respect to at least claim 12 (e.g. the use of cascoded current mirrors, with their cascaded pairs of transistors), and the same reasoning as described above with respect to at least claims 13-14, and 17 (e.g. adding Oda's first/second elements to the output of Kraus' circuit), claim 19 is rendered obvious. The cascaded pairs of transistors would provide a known means for allowing operation with higher power supply voltages, more stable current, and/or for generating a lower output voltage. Oda's first/second elements would provide a known means for removing noise from the output of a band gap circuit (one known type of reference voltage generating circuit). By replacing first element R1 with a transistor to allow means to adjust the filtering characteristics of the first/second elements, claim 27 is rendered obvious. Also, since switching element M5 is an N-channel transistor, claim 29 is rendered obvious.

No claim is allowable as presently written.

Allowable Subject Matter

Claims 1 and 5 would both be allowable if satisfactorily rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the second element, having a capacitive component, comprises an ion implantation resistor as recited within claims 1 and 5. However, the relationships between the first/second elements and the other components recited within the claims must be clarified.

Claims 3, 6, 8-9, 15, 21, 25, and 28 would also be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. Claims 3 and 8 both carry over the rejection from claim 1, and claims 6 and 9 carry over the rejection from claim 5. Claims 15, 21, 25, and 28 carry over the rejection from claims 13, 17, 23, and 19 respectively. However, similar to claims 1 and 5, there is presently no strong motivation to modify or combine any prior art reference(s) to ensure the second element, having a capacitive component, comprises an ion implantation resistor as recited within each of claims 15, 21, 25, and 28.

Prior Art

The other prior art references on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Fig. 1 of Ochi shows a band gap circuit comprising switching element M11 for discharging excess current to a reference point (e.g. see column 5, lines 42-45), but that excess current is from current source 11, and not from the circuit output terminal at VREF. Giuroiu shows/disclose an example of cascoded current mirrors 210 in Fig. 2 providing current to differential amplifier 105. Guo et al. shows a voltage regulating circuit, and

teaches the concept of using an ion implantation resistor to minimize process variations of its resistance (e.g. see column 3, lines 53-58). Therefore, these references should be reviewed and considered with respect to the basic limitations recited within the present application's claims.

The two references cited on the IDS were reviewed and considered. Although not used in any formal rejection described in this Office Action, patent 210414 from Taiwan was found to correspond to U.S. Patent 5,229,710 (i.e. Figs. 1-5 of each reference matches each other by structure and reference designators) found during a recent update search. Therefore, the U.S. reference was cited in the formal rejections.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund
6 Aug 2005

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PRIMARY EXAMINER
8/8/05